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DETERMINATION OF TECHNOLOGICAL PARAMETERS OF DRIFT TRANSISTORS ACCORDING TO SPECIFIED OPERATIONAL CHARACTERISTICS

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Algorithm of determination of physical parameters of a transistor structure for obtaining a specified set of its basic electrical characteristics has been presented. Empirical formulas derived by statistic processing of a large quantity of experimental data which allow to determine parameters of structure of drift n-p-n-transistor with the most optimum combination of output characteristics have been used for building the algorithm.

Existing methods and computation algorithms of bipolar transistors both discrete as well as bipolar chip elements assume carrying out of calculation of electric parameters and characteristics of transistors on the basis of known modes of the basic technological operations in the following sequence: known technology - parameters of impurity distribution - electric parameters and characteristics. However, during real designing of transistors - either the best foreign analogs or as the elements of microchips – its electric parameters and characteristics are known or given, and technology regarding the modes of technological operations represents "know-how". In that case a usage of known methods and algorithms of computation demands searching a great number of variants of modes of technological operations to obtain a demanded set of parameters and characteristics. It demands significant expenditures of time even using computer facilities as well as very high qualification of the developer, based on large practical experience and developed intuition. But even under these conditions the set of electric parameters and characteristics of transistors often is not optimal for the chosen variant of technology.

It is known, that drift transistors have the best set of parameters, but its calculation is more difficult and longer, than for diffusion transistors.

With the purpose of reduction of time for development of drift transistors and bipolar microchips as well as for obtaining of optimal set of parameters and characteristics of transistors it is necessary to apply the calculation method in the following sequence: electric parameters and characteristics - parameters of impurity distribution - modes of technological operations.

The investigations carried out (including the present work) allow to offer following computation algorithm of drift n - p - n transistors using new method:

The task for carrying out of the calculations includes:

- minimum amplification coefficient - B_{Nmin};
- maximum amplification coefficient - B_{Nmax};
- emitter-base breakdown voltage V_{ebo};
- collector-base breakdown voltage V_{cbo};
- collector-emitter breakdown voltage V_{ceo};
- the mode for the measurement of parameters – V_k and I_k (collector voltage and current).

Parameters of impurity distribution in the drift transistor are:

- impurity concentration at the emitter-base p-n-junction N_{eb};
- impurity concentration at the collector-base p-n-junction N_{cb};
- emitter depth (emitter-base p-n-junction depth) X_{je};
- base depth (collector-base p-n-junction depth) X_{jb};
- thickness of high-resistance collector W_c;

The calculation of impurity distribution parameters consists of three steps:

- calculation of parameters of collector-base junction (N_{cb}, X_{jb}) and concentration N_{eb};
- calculation of additional values;
- computation of base thickness W_{bo}, emitter depth X_{je} and thickness of high-resistance collector W_k.

Computation algorithm on the first step includes:

- calculation of the coefficient showing the difference of diffusion p-n-junction from the abrupt one by avalanche breakdown voltage χ_F [1]

$\chi_F = 1+3.6 \cdot 10^{-4} (V_{ebo})^{2.54}$;

- calculation of impurity concentration at the emitter-base junction [2]

$$N_{eb} = \sqrt{\left[\frac{2.7\cdot 10^{12}}{V_{ebo} - \frac{10}{(V_{ebo})^{0.72}}}\right]^3} ;$$

- calculation of the avalanche breakdown voltage of the collector-base p-n-junction $V_{cbo.a}$ [3]:

$V_{cbo.a.} = V_{ceo} \cdot \sqrt[4]{B_{N\max} + 1}$;

- calculation of specific resistance of an epitaxial layer ρ_{ep} [4]:

$$\rho_{ep} = 4.8 \cdot 10^{-4} \left(\frac{V_{cbo.a.}}{\chi}\right)^{1.92}$$

- rounding of value ρ_{ep} to the magnitude corresponding to technical specification for epitaxial structures and assignment of ρ_{ep} for further calculations in the interactive mode;

- calculation of breakdown voltage of the flat area of p-n-junction $V_{br.fl.}$ [5]:

$V_{br.fl.} = 86 \cdot \rho_{ep}^{0.64}$;

- calculation of impurity concentration at the collector-base p-n-junction N_{cb} [6]:

$$N_{cb} = \sqrt{\left[\frac{2.7\cdot 10^{12}}{V_{br.fl.} - \frac{10}{(V_{br.fl.})^{0.72}}}\right]^3} ;$$

- calculation of base region depth X_{jb} (the depth of collector-base junction) [4]

$$X_{jb} = 0.144 \cdot \left(\frac{V_{cbo.a.}}{\chi}\right)^{0.7} \cdot 10^{-4} ;$$

- rounding of the obtained value X_{jb} and adding to it a margin of 0.1÷0.3 μm (for the usage in technical documentation and further calculations in the interactive mode).

Computation algorithm on the second step includes:

- calculation of contact potential difference at collector and emitter junctions [7]:

$$\varphi_{cc} = \frac{KT}{e}\ln\frac{N_{cb}^2}{n_i^2}; \qquad \varphi_{ec} = \frac{KT}{e}\ln\frac{N_{eb}^2}{n_i^2};$$

- calculation of carrier mobility next to emitter (by N_{eb}) and collector p-n-junctions [8]:

$$\mu_n = \frac{1265}{1+\left(\frac{N}{8.5\cdot 10^{16}}\right)^{0.72}} + 65, \qquad \mu_p = \frac{447}{1+\left(\frac{N}{1.9\cdot 10^{16}}\right)^{0.76}} + 47;$$

- calculation of diffusion coefficient next to emitter and collector p-n-junction D_{ne}, D_{nc}, D_{pe}, D_{pc} [7]:

$$D = \frac{KT}{e}\cdot\mu;$$

- calculation of the life time τ_{ne}, τ_{pe}, τ_{nc}, τ_{pc} [9]:

$$\tau_p = \frac{\tau_{po}}{1+\frac{N}{7.1\cdot 10^{15}}}; \qquad \tau_n = \frac{\tau_{no}}{1+\frac{N}{8\cdot 10^{15}}};$$

- calculation of carrier diffusion length L_{ne}, L_{pe}, L_{nc}, L_{pc} $(L = \sqrt{D\cdot\tau})$ [5].

Computation algorithm on the third step includes:

- calculation of averaged impurity concentration in base $N_{b.av.}$ [10]:

$$N_{b.av.} = \exp\left\{\frac{\ln\cdot(N_{eb}\cdot N_{cb})}{\left[2-\frac{\ln(\frac{N_{eb}}{N_{cb}})}{2\cdot\ln(N_{eb})}\right]}\right\};$$

- calculation of minimum base thickness $W_{b.\min}$ [10]:

$$W_{b.\min} = \sqrt{\frac{2\varepsilon\varepsilon_0(V_{ceo}+\varphi_{cc})}{eN_{b.av}}};$$

- calculation of maximum base thickness $W_{b.\max}$ [11]:

$$W_{b.\max} = \sqrt{\frac{D_{ne}\tau_{pe}\left(V_{ceo} + V_c + \varphi_{cc}\right)}{1.2B_{N\min}\left(V_{ceo} + \varphi_{cc}\right)}} \cdot \ln\left(\frac{N_{eb}}{N_{cb}}\right);$$

- calculation of average base thickness $W_{b.av.}$:

$$W_{b.av.} = \frac{W_{b.\max} + W_{b.\min}}{(2 \div 2.15)};$$

- rounding the value of technological thickness of base $W_{b.av}$, taking it for further calculations and putting it into technical documentation W_{bo} (in the interactive mode);

- calculation of emitter depth $X_{je} = X_{jb} - W_{bo}$;

- calculation of high-resistance collector thickness [12]:

$$W_c = \sqrt{\frac{2\varepsilon\varepsilon_0\left(V_{cbo} + \varphi_{cc}\right)}{eN_{cb}}}.$$

Thus, the parameters of impurity distribution N_{cb}, N_{eb}, X_{je}, X_{jb}, W_k are determined in the process of calculations.

The method offered for calculation of impurity distribution parameters in the drift n-p-n transistor allows to determine an impurity distribution in the base region and to estimate the thickness of a high-resistance collector W_c with sufficient degree of accuracy.

However, a real breakdown by overlapping which determines breakdown voltage V_{cbo} does not occur when the depth of space-charge region (SCR) of a collector-base junction becomes equal to the thickness W_c, but when SCR reaches some point **A** (fig.1) being in the region of diffusion of an n^+-hidden layer (for bipolar microchips).

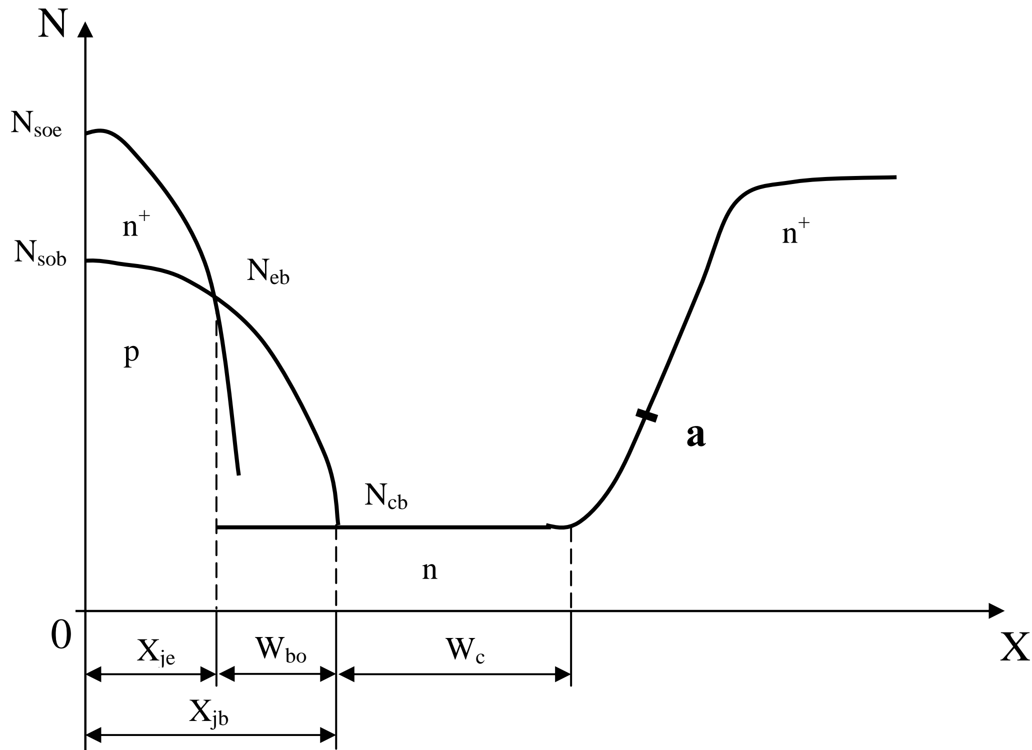

Fig.1. Impurity distribution in the drift n-p-n transistor.

Up to the present time there is no technique of the accurate enough determination of the overlap voltage by the impurity distribution in the regions of n^+-layer diffusion, though this is an actual problem for both transistors as well as diodes. The absence of such a technique affects especially strongly devices of SHF range as well as high-power devices.

An excess distance in the region of high-resistance collector leads to occurrence of an additional resistance which reduces working frequency and results in a saturation voltage that conducts to excess dissipated power in the device, to the overheat and reliability degradation. Thus the problems of obtaining of preset diffusion of layers in the technological process, calculation of impurity distribution in it as well as calculation of the overlap voltage in the region of diffusion are still actual.

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