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C_2 MODEL OF THE WIDE-BANDGAP MOSFET

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Abstract. A new MOSFET segmented model is proposed. In the model, the current in saturation is not considered independently, but as an extrapolation of the current of the physical model in the unsaturated (linear) mode by Padé approximant. The first two coefficients of the approximant are determined from the condition of continuity of the transistor current at the boundary of the saturated region along with two derivatives; the remaining coefficients are determined by parametric optimization based on measured current-voltage characteristics. This saturation current model is invariant with respect to the model for the unsaturated mode and the physics of processes at current saturation. This model was created primarily for simulating transistors manufactured using various wide-gap semiconductor technologies: silicon carbide, gallium nitride and diamond. The results of modeling GaN and SiC transistors with low root mean square error are presented. The RMS error of the models does not exceed 3%.

Key words: silicon-carbide (SiC), gallium-nitride (GaN), diamond (C), modeling, wide-bandgap MOSFET, C_2-continuity, parameter extraction.

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Introduction

Wide-bandgap (WBG) devices, such as silicon carbide (SiC), gallium nitride (GaN), and diamond (C) metal oxide semiconductor field-effect transistors (MOSFETs), are the promising alternatives that replace conventional silicon (Si) power devices [1-6]. Significant improvements in the quality of GaN and SiC materials over the past few years have meant that design optimization using circuit simulators based on compact power MOSFET models is playing an increasingly important role.

The main disadvantage of regional models is considered to be the break in continuity in characteristics' higher derivatives. When the second derivative breaks, the third derivative becomes uncontrollably large and digital noise appears when numerically solving the differential equations of a circuit when analyzing transient processes. Such noise can be observed directly in the spectral characteristics of RF circuits using C_1 (a function is C_n-continuous if the function and its first n derivatives are continuous) Shichman-Hodges model.

To obtain a regional C_∞-continuous model, smoothing functions are usually used. This method does not solve all problems, since the use of smoothing leads to an increase in model error. It is possible to select the parameters of the smoothing function in such a way that the increase in error is minimal. However, at the same time, higher derivatives of characteristics begin to grow rapidly, destroying the advantages of smoothing.

The requirement of C_∞-continuity of circuit component models is desirable, but spare, since many C_1-continuous models are successfully used in simulators [3]. The industry-standard BSIM-BULK MOSFET model uses Hermitian interpolation by the polynomial of the seventh order, to wit, is C_3-continuous [7].

This paper introduces the new compact DC models SiC and GaN MOSFETs, which are an evolution of the silicon power MOSFET model [8]. The continuity of the model, together with its first two derivatives, makes the numerical methods used in simulators efficient. The model features an accurate description of the MOS channel and the gradual transition of drain current from linear to saturation region with increasing drain bias by Padé approximant. To simulate such an intermediate area,

the physical complicated model uses an internal node and internal iterations for calculate its voltage [9].

The ease of parameter extraction is essential property of MOSFET models, sins the applicability of a MOSFET model in circuit simulation is highly dependent on how easily and accurately the model parameters can be extracted. In this work we have use nonlinear global least squares optimization, which gives the minimum average error between calculated and measured results and is commonly used technique in parameter extraction.

The small number of model parameters allowed them to be identified using a standard least squares program that minimizes the mean square error. Solving the least squares problem is difficult with an ill-conditioned Hessian matrix. The Hessian describes the curvature of the objective function. Poor conditioning means that the objective function has a ravine with steep sides but a very flat bottom. This makes it difficult to quickly move down the ravine. As a result, some of the determined parameters lose accuracy. Typically, the condition number of a Hessian increases greatly as the model error decreases and/or the number of model parameters increases. For this reason, standard least squares programs do not always satisfy the practical needs of parametric optimization [10, 11]. With a ravine structure of the objective function, fast gradient least squares methods are effective only when the function dimension is small. In the proposed models, the number of new parameters determined by measurements is minimal.

This manuscript is organized as follows. Section 1 describes the simple C_2 MOSFET model and provides an example of the implementation of the simplest model in the form of an LTspice subcircuit. Section 2 shows that adding two new terms to the Padé approximant significantly improves the original model when applied to SiC MOSFETs. Section 3 gives the GaN MOSFET model obtained by both linear-region current extrapolation and saturation-region interpolation of measured data. Section 4 presents the results of the diamond transistor simulation. Section 5 describes an assessment of the possibility of further refinement of the C_2 model and presents the conclusions drawn from this work.

1. C_2 extrapolation MOSFET model

The regional (segmented) model of MOSFET has the form

$$I_D = \begin{cases} 0, \ V_{GS} < V_{TH} \\ I_1, V_{DS} < V_{SAT} \\ I_2, V_{DS} \geq V_{SAT} \end{cases}, \quad (1)$$

where I_D is a drain current; V_{GS} and V_{DS} are gate-source, drain-source voltage, respectively; V_{TH} denotes a threshold voltage; V_{SAT} is a drain saturation voltage. For long channel MOSFET, in most models V_{SAT} is determined by channel pinch-off at the drain side of channel.

If we neglect the effects of saturation of charge carrier velocity and space charge, we can estimate I_D in the nonsaturation (linear) region as:

$$I_1(V_{GS}, V_{DS}) = \frac{\beta_0}{1+\theta(V_{GS}-V_{TH})}\left(V_{GS}-V_{TH}-\frac{1}{2}V_{DS}\right)V_{DS}, \quad (2)$$

where β_0 is the conduction coefficient; θ is the mobility degradation coefficient due to vertical field [12].

As the drain voltage approaches the cutoff voltage, the gradual channel approximation is violated and (2) loses its consistency [13]. Therefore, in what follows, the maximum drain voltage in (2) is considered to be the saturation voltage $V_{SAT} = k(V_{GS} - V_{TH})$, where k is a coefficient determined by measurement ($0 < k < 1$).

In saturation region, the transistor current increases monotonically and nonlinearly. This requirement is satisfied by the truncated Padé approximant as:

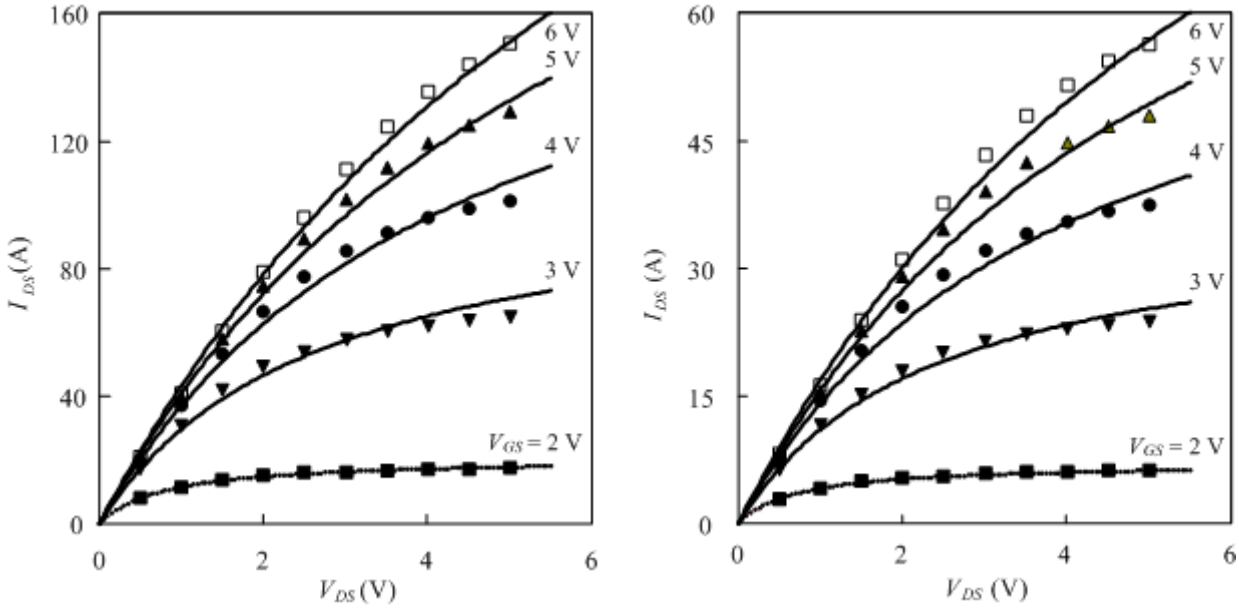
$$I_2 = I_1(V_{GS}, V_{SAT})\frac{1+a_1(V_{DS}-V_{SAT})}{1+b_1(V_{DS}-V_{SAT})}. \quad (3)$$

Parameters a_1 and b_1 of (3) can be expressed in terms of the parameters $I_1(V_{GS}, V_{DS})$ from the conditions of continuity of the current and its first and second derivatives at $V_{DS} = V_{SAT}$ as:

$$b_1 = -\frac{1}{2}\frac{\partial^2 I_1}{\partial V_{DS}^2}\bigg|_{V_{SAT}} \Bigg/ \frac{\partial I_1}{\partial V_{DS}}\bigg|_{V_{SAT}}, \quad a_1 = b_1 + \frac{\partial I_1}{\partial V_{DS}}\bigg|_{V_{SAT}} \Bigg/ I_1(V_{GS}, V_{SAT}).$$

Note that the coefficients a_1 and $b_1$are obtained explicitly. Thus, using the new parameter k, it is possible to obtain the current of model in the saturation region only by extrapolation. The peculiarity of model (1)-(2)-(3) is that its parameters are determined only jointly by the least squares method. The model (3) has a simple description of the channel current accurately reproduce the gradual transition from linear to saturation seen in power MOSFETs

The measured and simulated output characteristics of the GaN power *n*-channel MOSFET at 25 ℃ and 150 ℃ are shown in Fig. 1. A reasonable agreement was achieved between the proposed model and the datasheet.



a *b*

Fig. 1. Comparison of output characteristics between model (1)-(2)-(3) (lines) with GaN power *n*-channel MOSFET GS66516T datasheet (marks) at 25 °C (a) and 150 °C (b).

In order to add quantitative analysis for comparison, specific accuracy metrics are required. In this study, RMS error is selected as the principal figure of merit for evaluating the accuracy of each model under consideration. This figure of merit is calculated from equation

$$E = \sqrt{\frac{1}{n}\sum_{j=1}^{n}\left[\left(I_{Dj}^{meas} - I_{Dj}^{sim}\right)\Big/ I_{Dj}^{meas}\right]^2},$$

where n is the number of data points, I_D^{meas} is the drain current measured in experiment, and I_D^{sim} is the drain current predicted by simulation. The choice of relative error $\delta_j = \left(I_{D\,j}^{meas} - I_{D\,j}^{sim}\right) \Big/ I_{D\,j}^{meas}$ allows one to compare the errors of different models for different transistors. The absolute error allows you to do the same only for a transistor of one type [3]. For solving curve-fitting problem, we used damped least-squares method based on the Levenberg–Marquardt algorithm with the error control by variation of initials. Table 1 shows the parameters and RMS error of models of MOSFETs. For SiC and GaN power MOSFETs, the ranges of V_{DS} and V_{GS} were selected according to the manufacturers' datasheets.

Table 1. Parameters and RMSE of models.

Транзистор	T_j (°C)	β_0 (A/B^2)	V_{TH} (B)	k	θ (1/B)	a_2 (1/B^2)	b_2 (1/B^2)	a_3 (1/B^3)	b_3 (1/B^3)	E (%)
SiC MOSFET LSIC1MO120G0040	25	2.660	6.708	0.4016	0.04076	–	–	–	–	2.86
	25	2.876	6.731	0.01274	0.03911	69.61	0.8722	–	–	1.66
	25	2.611	6.622	0.4886	0.03923	–	–	4.592 E-4	8.145E-4	2.75
SiC MOSFET C3M0016120R	25	11.27	5.156	0.06058	0.07389	–	–	–	–	1.70
	25	11.36	5.025	0.19723	0.07974	0.013806	2.322 E-4	–	–	1.38
	25	12.33	6.515	0.1778	0.2754	–	–	–	–	1.85
SiC MOSFET C2M0026120D	25	12.41	6.499	0.01054	0.2715	150.7	1.062	–	–	1.76
	150	30.49	3.815	0.2043	1.44	–	–	–	–	2.64
	150	19.57	4.251	1E-9	0.8839	1.611E-5	1.615E-3	–	–	1.91
GaN MOSFET GS66516T	25	122.6	1.580	0.04648	2.299	–	–	–	–	3.98
	25	150.7	1.561	0.1760	3.045	–	–	0.3966	0.677	2.36
	25	116,5	1.584	0.00269	2.156	98.41	0.1456	–	–	3.92
	150	40.42	1.559	0.1222	1.908	–	–	–	–	3.98
	150	55.45	1.577	0.2106	2.868	–	–	0.6574	1.4509	2.23

Below is a subcircuit for model (1)-(2)-(3):

```
.SUBCKT MOSFET S1 S2 S3
* Institute for Radio Engineering Systems and Control, Taganrog
* Model Universal C2. Format: LTSPICE
* Node S1 -> Drain
* Node S2 -> Gate
* Node S3 -> Source

.PARAM B0=122.6 VT=1.580 k=0.04648 THETA=2.299   ; GS66516T, T=25 C

EG   G   0  VALUE={(ABS(V(S2) - V(S3) - {VT}) + V(S2) - V(S3) - {VT}) / 2}
ES   S   0  VALUE={V(G) * {k}}
E1   DD  0  VALUE={(V(S1) - V(S3) - V(S) - ABS(V(S1) - V(S3) - V(S))) / 2 + V(S)}
E2   DS  0  VALUE={(V(S1) - V(S3) - V(S) + ABS(V(S1) - V(S3) - V(S))) / 2}
G0   IS  0  VALUE={((V(G) - V(DD) / 2) * V(DD))}
V0   0   IS 0
EB   B   0  VALUE={1 / 2 / (V(G) - V(S))}
EA   A   0  VALUE={V(B) + (V(G) - V(S)) / I(V0)}
G1   S1  S3 VALUE={{B0} * I(V0) * (1 + V(A) * V(DS)) / (1 + V(B) * V(DS)) / (1 +
{THETA} * V(G))}

* Intrinsic body diode
D1   S3  S1 IBD
.MODEL IBD D (IS=2E-12 N=1 RS=0.1 CJO=1E-9 BV=1200 TT=0.1U)
.ENDS
```

2. C_2 model of SiC MOSFET

Unlike silicon, SiC power MOSFETs have a large gradual transition between linear and saturation region, which is due to a combination of low resistance of the drift region and significant density of interface states in the inversion channel [9, 14]. Extrapolation of I_1 to the saturation region according to (3) cannot take into account this feature of the SiC MOSFET and therefore the I_2 equation must contain parameters associated with the measured current values in the saturation region near V_{SAT}.

Obviously, to improve the accuracy in the saturation region, in which the output characteristics of SiC transistors are qualitatively different from the characteristics of Si ones, it is necessary to take the Padé approximant with an increased number of terms. For example, as:

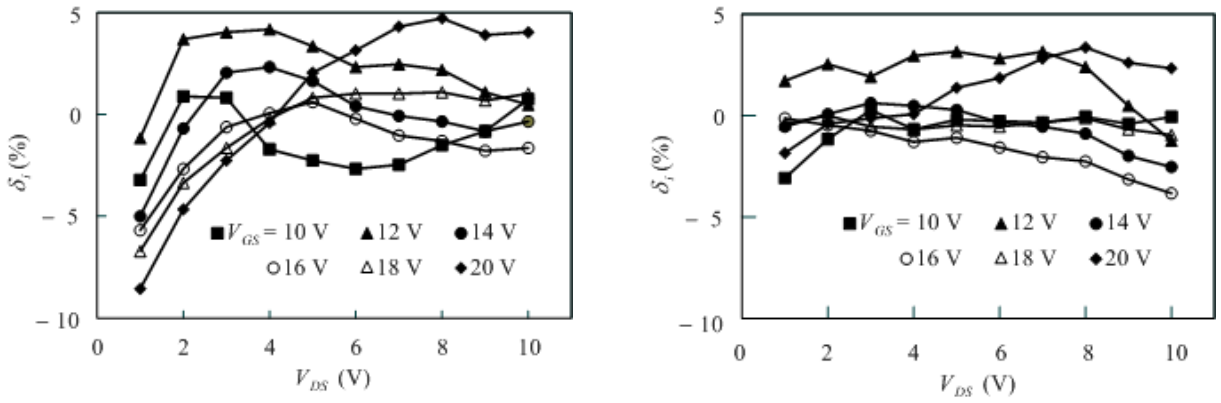
$$I_2 = I_1(V_{GS}, V_{SAT}) \frac{1 + a_1(V_{DS} - V_{SAT}) + a_2(V_{DS} - V_{SAT})^2}{1 + b_1(V_{DS} - V_{SAT}) + b_2(V_{DS} - V_{SAT})^2}. \quad (4)$$

Here, the coefficients a_1 and b_1 are still determined from the condition of continuity of the current and its first two derivatives at $V_{DS} = V_{SAT}$. The difference from the previous case is that coefficient b_1 depends not only on the parameters of I_1,

but also on the new coefficients a_2 and b_2:

$$b_1 = \left[(a_2 - b_2) I_1(V_{GS}, V_{SAT}) - \frac{1}{2} \frac{\partial^2 I_1}{\partial V_{DS}^2}\bigg|_{V_{SAT}} \right] \Bigg/ \frac{\partial I_1}{\partial V_{DS}}\bigg|_{V_{SAT}} .$$

The most common model validation technique is graphical overlay of experimental data and simulation predictions for static I-V curves. When the error is small and/or the range of currents is large, to demonstrate the effectiveness of the approximation, it is convenient to consider not the graphs of the approximated and approximating functions, but the graph of their difference. Figure 2 shows that model (1)-(2)-(4) allows the RMS error to be reduced, and the maximum error is reduced even more. A similar graphical description of the modeling error is used in [15], but Fig. 2 allows one to obtain a complete picture of the error over the entire range of control voltages.



a *b*

Fig. 2. Residuals of model (1)-(2)-(3) (*a*) and (1)-(2)-(4) (*b*) for SiC power *n*-channel MOSFET LSIC1MO120G0040. T_j = 25 °C.

Replacing model (1)-(2)-(3) with model (1)-(2)-(4) leads, as Table 1 shows, to a decrease in the RMS error by an average of 20%.

3. C_2 model of GaN MOSFET

As Table 1 shows, model (1)-(2)-(4) for a GaN transistor has no advantages over (1)-(2)-(3). This can be explained by the fact that the introduction of coefficients a_2 and b_2 makes it possible to clarify the current I_2 only at low drain voltages $V_{DS} \approx V_{SAT}$. Adding new terms with coefficients a_3 and b_3 is also ineffective. To reduce the error,

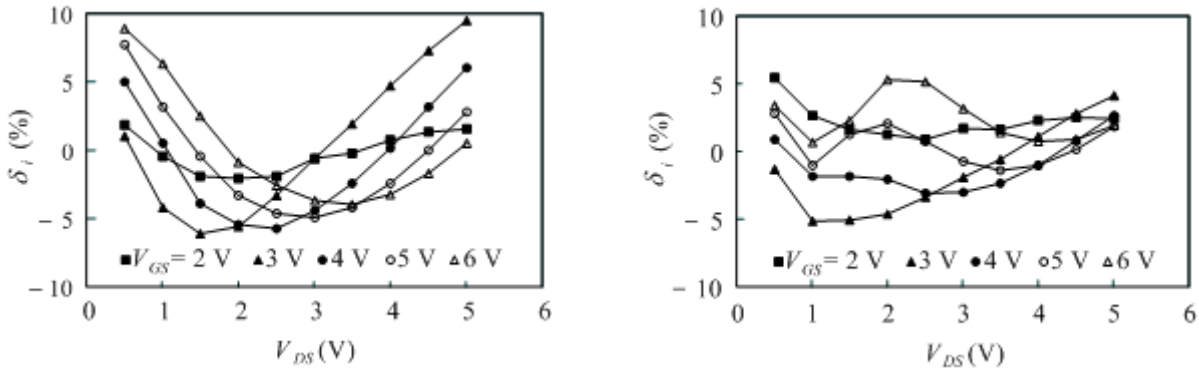
we supplement extrapolation with interpolation. Let us add a new supplement to function (3), the first two derivatives of which at $V_{DS} = V_{SAT}$ are equal to zero:

$$I_2 = I_1(V_{GS}, V_{SAT})\left[\frac{1+a_1(V_{DS}-V_{SAT})}{1+b_1(V_{DS}-V_{SAT})}+\frac{a_3(V_{DS}-V_{SAT})^3}{1+b_3(V_{DS}-V_{SAT})^3}\right]. \quad (5)$$

Here the coefficients a_1 and b_1 are determined in exactly the same way as in (3), and the new coefficients a_3 and $b_3$are determined independently by parametric optimization.

Figure 3 shows that the error of model (1)-(2)-(5) decreases compared to (1)-(2)-(3), and most strongly in the region of high drain voltages. Note that Figures 3*a* and 1*a* present the same table of measured and simulated currents.

As Table 1 shows, using model (5) instead of (3) has nearly no effect on the error value and parameters of SiC MOSFET, which confirms the special properties of the I-V characteristics of this transistor in the saturation region.



a *b*

Fig. 3. Residuals of model (1)-(2)-(3) (*a*) and (1)-(2)-(5) (*b*) for GaN power *n*-channel MOSFET GS66516T. T_j = 25 °C.

As can be seen from Table 1, the coefficient θ, which determines the degradation of charge carrier mobility in a transverse field, is significantly greater for GaN MOSFETs than for SiC. With increasing θ, parametric optimization becomes unstable, that is, changes in the initial conditions for optimization lead to large changes in the parameters β_0 and θ with very small changes in the objective function, as a result of which model (1)-(2)-(5) becomes unsuitable. In such cases, instead of model (2), one should try a more accurate model [8], used for high-voltage Si MOSFETs, in which the

mobility of charge carriers depends not on the gate to source voltage, but on the gate to channel voltage varying along the channel:

$$I_1 = \beta_0 V_K \left[V_{DS} - V_K \ln\left(\frac{V_K + V_{GS} - V_{TH}}{V_K + V_{GS} - V_{TH} - V_{DS}} \right) \right], \quad (6)$$

were V_K is an empirical constant ($V_K \approx 1/\theta$). Examples of using model (1)-(3)-(6) are given in Table 2.

Table 2. Parameters of model (1)-(3)-(6) for GAN MOSFETs; T_j = 25 °C.

MOSFET	β_0 (A/V^2)	V_{TH} (V)	V_K (V)	k	RMSE (%)
GS66516T	58.72	1.256	0.8110	0.5971	5.66
GS65508B	155.2	1.246	0.7673	0.7673	2.48

From Table 2 and the results obtained in [8], it follows that the V_K parameter of a GaN MOSFET is significantly less than that of a Si one, that is, the electron mobility in the GaN MOSFET channel depends on the transverse field more strongly than that of a Si MOSFET. This difference is all the more convincing if we note that the maximum gate voltage for a Si MOSFET was 30 V, and for a GaN only 6 V.

The currents determined by (2) and (6) are very close to each other, but their derivatives and, consequently, the coefficients a_1 and b_1, can differ greatly as θ increases. For this reason, model (5), which is compatible with (2), is not compatible with (6).

4. C_2 model of MOSFET on monocrystalline carbon

Field-effect transistors based on diamond are not currently mass-produced. However, to evaluate their properties, it is useful to obtain their C_2 model parameters. For the output characteristics of a *p*-channel transistor with a channel width of 6.6 μm and a length of 7.17 μm for model (1)-(2)-(3), the following parameters were obtained: β = 5.58 μA/V, V_{TH} = – 1.23 V, k = *0.794*, θ = 0.0401 V^{-1}. Fig. 4 shows the distribution of model errors at the points of I–V characteristic measurements.

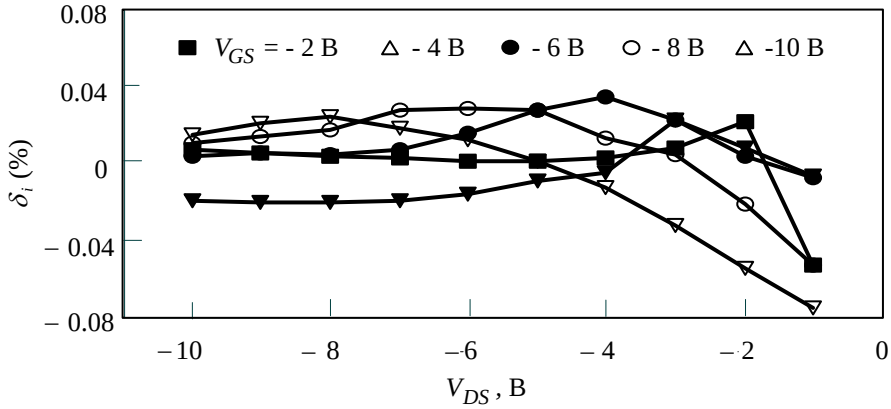


Fig. 4. Distribution of errors of models (1)-(2)-(3) for a *p*-channel diamond transistor [6]. T_j = 25 °C.

Discussion and conclusions

C_2 models have the main disadvantage of regional models: lack of robustness, which is manifested in the fact that there is a probability of the model having a negative output resistance (more precisely, this disadvantage is not a property of the model, but of the method of extracting its parameters). For example, at low temperatures, the Shichman-Hodges model has this property [16]. To prevent such a situation, parametric optimization should be carried out with the constraint k < 1.

The initial region of the output characteristics of the transistor, corresponding to the current I_1, can be so small that almost all the I-V characteristics are described by the I_2 model. This situation is often observed with increasing temperature. Accordingly, the parameter k can be so small that its value becomes commensurate with the error in its identification, that is, the parameter k can be not only small, but also negative. To prevent such a situation, optimization should be carried out with the constraint $k > 0$. For example, for the transistor C2M0026120D at 150 °C $k \approx 10^{-9}$ (see Table 1). It is important to note that even at $k \approx 0$, the C_2 model remains semi-physical and the parameters β_0, V_{TH}, and θ retain their physical meaning since, although the function (2) itself is not used in calculating the current, its derivatives continue to be used. All parameters of the above models are determined jointly, therefore, with a further increase in the dimension of the Padé function, the error of the models decreases insignificantly, being limited by the error of the model of the initial region of the I-V characteristic. In addition, with an increase in the number of terms in the Padé function,

which may be necessary to reduce the error in modeling the output conductivity, the probability of the appearance of zeros and poles outside the considered range of voltages V_{GS} and V_{DS} increases, which is unacceptable for compact models.

Model (2) and, to a lesser extent, (6) do not provide high accuracy of modeling the small-signal gate transconductance $\partial I_D/\partial V_{GS}$. To improve it, it is necessary to more accurately approximate the dependence of the charge carrier mobility in the channel on the gate field.

A new semi-physical simple, but at least no less accurate in comparison with the known compact models of field-effect transistors on wide-gap semiconductors has been presented in this paper. The transistor current in saturation is approximated by the Padé function, which allowed us to accurately describe the smooth transition to the saturated mode observed in SiC transistors. The models are developed for use in electronic simulators and retain all the advantages of the original physical models in the unsaturated region of the current-voltage characteristic with high accuracy in the saturation region. Particular attention in the work was paid to the simplicity and reliability of the procedure for identifying the model parameters, which relies on device data available in device datasheets.

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